Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method, comprising:

synchronising start of cell times in input/output circuits with cell transmission periods in a cross-connection ~~circuit,~~ circuit;

transferring cells between said input/output circuits by said cross-connection circuit in cell transfer ~~periods,~~ periods;

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration ~~periods,~~ periods;

sending cells from a sending input/output circuit of said input/output circuits at start of cell ~~times,~~ times;

receiving said sent cells in said cross-connection ~~circuit,~~ circuit;

oscillating between a loopback configuration and a no-transmission ~~configuration,~~ configuration;

transferring the received cells back to said sending input/output circuit in said loopback configuration and not transferring the received cells back to said sending input/output circuit in said no-transmission ~~configuration,~~ configuration;

receiving back transferred cells in said sending input/output circuit during said loopback ~~configuration,~~ configuration;

checking said cells transferred back during said loopback configuration in said sending input/output circuit for a transmission ~~error,~~ error; and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

2. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of start of cell times in said sending input/output circuit, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

3. (Previously Presented) A method according to claim 1, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

4. (Previously Presented) A method according to claim 1, including calculating start of cell times based on a start of cell signal and said offset of said start of cell times, serializing said cells, and sending said serialized cells together with said start of cell signal at said start of cell times.

5. (Previously Presented) A method according to claim 1, including receiving transferred back cells, de-serializing said cells and checking each cell for transmission errors.

6. (Previously Presented) A method according to claim 1, including receiving transferred back cells, de-serializing said cells and evaluating a bit error indicator.

7. (Previously Presented) A method according to claim 3, wherein the shifting includes shifting said offset of start of cell times using an offset counter and changing said offset counter by an amount of clock cycles of said central clock signal.

8. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of said start of cell times to a maximum without generating transmission errors, and shifting said offset of said start of cell times to a minimum without generating transmission errors.

9. (Previously Presented) A method according to claim 8, wherein the shifting includes setting said offset of said start of cell times in between said maximum and said minimum.

10. (Currently Amended) A packet switch comprising:

a plurality of port controllers each with a cell input port and a cell output port, the cell output ports configured to output cells at respective start of cell times; and

a cross-connection ~~means~~ switch including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a sending port controller of said port controllers comprises:

an error detector configured to detect corrupt received cells; and

~~a start of cell signal generator for generating start of cell signals,~~

an offset controller ~~for shifting a~~ configured to shift the start of cell ~~time~~ times for the respective output port ~~based on said start of cell signal,~~ in response to the detection of corrupt received cells by the error detector; and

~~an error detection means for detecting corrupt received cells,~~

wherein said cross-connection ~~means~~ switch comprises:

a configuration controller ~~for controlling~~ configured to control an oscillation of the cross-connection switch between a loopback configuration in which cells received by the cross-connection switch are transferred back to a respective sending port controller, and a no-transmission configuration of said cross-connection switch. ~~means and the offset controller is configured to adjust the start of cell time based on detected corrupt cells received during the loopback configuration.~~

11. (Currently Amended) A packet switch according to claim 10, further comprising a central clock generator for providing a central clock signal, wherein ~~said~~ each sending port controller comprises a start of cell signal generator, and said start of signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

12. (Previously Presented) A packet switch according to claim 10, wherein said sending port controller comprises a serializer and a de-serialize for serializing cells to be sent and de-serializing received cells.

13. (Currently Amended) A packet switch according to claim 10, wherein said cross-connection ~~means~~ switch comprises an ~~comprise a~~ N × N crossbar matrix, selectively connecting N cell input ports with N cell output ports.

14. (Currently Amended) A packet switch according to claim 13, wherein said loopback configuration is realized ~~realised~~ by a unit matrix and a no-transmission configuration is ~~realised~~ realized by a null matrix.

15. (Currently Amended) A packet switch according to claim 10, wherein said error ~~detection means~~ detector is a bit error indicator.

16. (Previously Presented) A method, comprising:

synchronizing start of cell times, in a packet switched network, for plural port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers;

transferring cells between said port controllers by said cross-connection circuit in cell transfer periods;

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods;

sending cells from a sending port controller of said port controllers at start of cell times;

receiving said sent cells in said cross-connection circuit;

oscillating between a loopback configuration and a no-transmission configuration;

transferring the received cells back to said sending port controller in said loopback configuration and not transferring the received cells back to said sending port controller in said no-transmission configuration;

receiving back transferred cells in said sending port controller during said loopback configuration;

checking said cells transferred back in said sending port controller for a transmission error; and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

17. (Canceled)

18. (Previously Presented) A method according to claim 16, wherein the shifting includes shifting said offset of start of cell times in said sending port controller, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

19. (Previously Presented) A method according to claim 16, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

20. (Currently Amended) A method, comprising:

synchronising start of cell times in a plurality of port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers, the port controllers each having a cell input port and a cell output port, the respective cell output ports of the respective port controllers configured to transmit cells at respective start of cell times, and the cross-connection circuit including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a respective sending port controller of said port controllers performs:

generating start of cell signals using a start of cell signal generator,

shifting a start of cell time for the respective port controller based on said start of cell signal using an offset controller, and

detecting corrupt received cells using an error detector, and

wherein said cross-connection circuit controls an oscillation between a loopback configuration in which data received from a respective sending port controller by the cross connection is transmitted back to the respective sending port controller, and a no-transmission configuration of said cross-connection circuit, using a configuration controller, and the shifting of the start of cell times for the respective port controllers is based on the detecting of corrupt cells ~~received during the loopback configuration.~~ transferred back to the respective port controllers.

21. (Previously Presented) A method according to claim 20, further comprising providing a central clock signal using a central clock generator, wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

22. (Currently Amended) A system, comprising:

a plurality of port controllers each having a cell input port configured to receive cells and a cell output ~~port;~~ port configured to transmit cells at start of cell times; and

a ~~cross-connection~~ cross-connection matrix coupled to the cell input ports and the cell output ports of the plurality of port controllers, the ~~cross-connection~~ cross-connection matrix having a configuration controller configured to control an oscillation of the cross-connection matrix between a loopback ~~configuration~~ configuration, in which data received by the cross-connection matrix is transferred back to a respective cell input port of the respective sending port controller, and a no transmission configuration, wherein a sending port controller of the plurality of port controllers comprises:

~~a start of cell signal generator configured to generate a start of cell signals;~~

an error detector configured to detect ~~errors in~~ corrupt cells ~~received during the loopback configuration;~~ transferred back to the sending port controller by the cross-connection matrix during the loopback configuration; and

an offset controller configured to shift a start of cell time for the sending port controller based on the detection of corrupt cells transferred back to the sending port controller by the cross-connection matrix ~~detected errors in the cells received~~ during the loopback configuration.

23. (Currently Amended) The system of claim 22, further comprising a central clock generator wherein the sending port controller comprises a start of cell signal generator and the start of cell signal generator, the offset controller, and the configuration controller are coupled to the central clock generator.

24. (Previously Presented) The system of claim 22 wherein the sending port controller comprises a serializer configured to serialize cells to be sent and a de-serializer configured to de-serialize received cells.

25. (Currently Amended) The system of claim 22 wherein the cross-connection matrix ~~comprise~~ comprises a N × N crossbar matrix configured to selectively connect N cell input ports with N cell output ports.

26. (Previously Presented) The system of claim 22 wherein the matrix is configured as a unit matrix in the loopback configuration and is configured as a null matrix in the no-transmission configuration.

27. (Previously Presented) The system of claim 22 wherein the error detector comprises a bit error indicator.

28. (New) The system of claim 22, wherein the offset controller is configured to select an offset to shift the start of cell time for the sending port controller so that the start of cell time is in a middle of a transmission time range, the transmission time range determined based on the detection of corrupt transferred back cells by the error detector.

29. (New) A method, comprising:

oscillating, during a set up period, a cross-connection switch coupled to a plurality of port controllers between a loop back configuration, in which data received by the cross-connection switch from a respective port controller in the plurality of port controllers is transferred back to the respective port controller, and a no-transmission configuration, in which data received by the cross-connection switch from the respective port controller is not transferred back to the respective port controller; and

determining, during the set up period, respective cell transmission time offsets for the plurality of port controllers by:

sending a cell from the respective port controller in the plurality of port controllers to the cross-connection switch at a transmission time based on a clock signal and a delay for the respective port controller;

checking data transferred back to the respective port controller by the cross-connection switch for receipt of a corrupt cell;

when receipt of a corrupt cell is detected, increasing the delay for the respective port controller;

repeating the sending, the checking and the increasing the delay for the respective port controller at least until receipt of a non-corrupt cell by the respective port controller is detected; and

setting the cell transmission time offset for the respective port controller based on the delay for the respective port controller.

30. (New) The method of claim 29, further comprising generating a central clock signal and providing the central clock signal to the plurality of port controllers and the cross-connection switch.

31. (New) The method of claim 30 wherein:

after receipt of a first non-corrupt cell by the respective port controller is detected, the sending, the checking and the increasing the delay are repeated until receipt of a subsequent corrupt cell by the respective port controller is detected; and

setting the cell transmission offset for the respective port controller comprises setting the transmission offset based on a value of the delay for the respective port controller when the first non-corrupt cell was received by the respective port controller and a value of the delay for the respective port controller when the subsequent corrupt cell was received by the respective port controller.

32. (New) The packet switch of claim 10 wherein the offset controller is configured to select an offset to shift the start of cell times for the respective sending port controller so that the start of cell times for the respective sending port controller is in a middle of a transmission time range, the transmission time range determined based on the detection of corrupt received cells by the error detector.